

# Simulations of electronic transport in ultra-thin and ultra-short junctionless transistors

Baruch Feldman



# Talk Overview

- Introduction / Motivation
- The Si nanowire junctionless transistor
  - Experimental background
  - Methodology
  - I-V curves
- The CNT junctionless transistor
  - I-V curves
- The TIMES transport code
  - As a benchmarking tool
- Conclusion

# “Short-channel effects”

- As Technology Roadmap reaches ~10 nm scale, everything changes
- Key issue: Gate’s ability to control electrostatics as channel gets shorter
  - “Short-channel effects”
  - In competition with source & drain for depletion charge

- Parameter: Length / Thickness
  - “Natural length” for circular cross-section

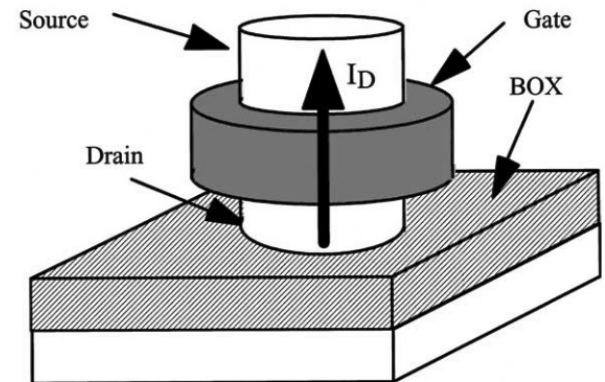
[Singh *et al*, IEEE - 2008]

- “Fancy” way of saying Length / Thickness
- More gates & thinner device → better gate control

$$\lambda = \sqrt{\frac{2\epsilon_{\text{si}}t_{\text{si}}^2 \ln\left(1 + \frac{2t_{\text{ox}}}{t_{\text{si}}}\right) + \epsilon_{\text{ox}}t_{\text{si}}^2}{16\epsilon_{\text{ox}}}}$$

(circular cross-section)

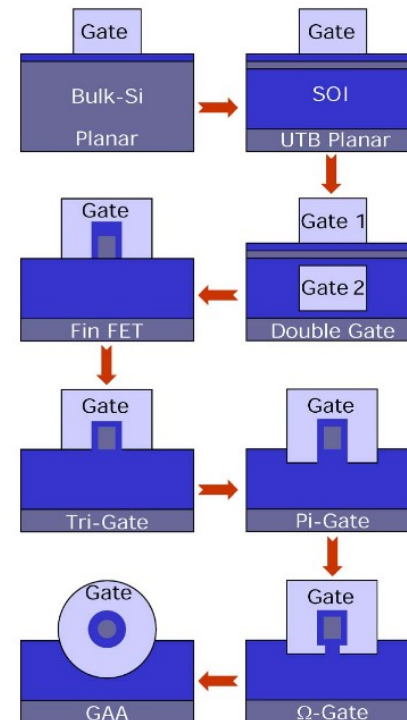
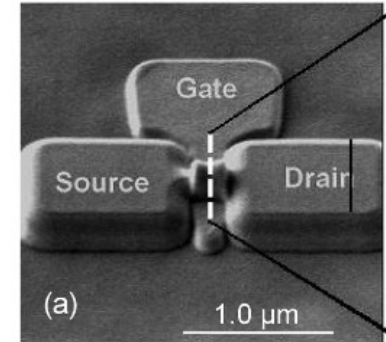
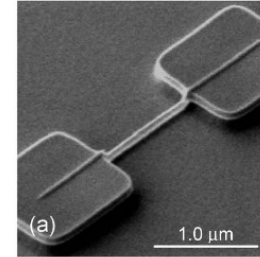
- Cylindrical geometry of gate-all-around (GAA) gives inverse log dependence of gate capacitance on channel diameter
  - So gate length can scale with wire thickness without reducing gate dielectric thickness [N. Singh *et. al*, IEEE Trans. Electron Device, 2008].



[Colinge, Solid-State Electronics, 2004]

# Proposed nanoscale devices

- Some Si nanowire (SiNW) devices already realized
  - Singh *et al* [*IEEE TED*, 2008] (figs. to right)
  - Junctionless SiNW transistor – Colinge *et al*
    - More soon – a major focus of this talk
- Tunneling FETs
  - Tunneling MOSFET
    - Hu *et al*, Berkeley
  - Tunneling nanowire FET
    - Tight binding models, Luisier, Klimeck
  - Poorly understood experimentally or theoretically
- Impact ionization FETs
  - Mayer *et al* [*IEEE EDL*, 2007]
- **ALL** devices face a major challenge from short channel effects
  - Response: Planar geometry → SOI → Multi-Gate → Gate-all-around (GAA) (fig. to right)
    - Thinner devices
  - *Junctioned* designs also face thermal budget / fabrication challenges



All figs. from [Singh *et al*, *IEEE TED*, 55, 3107 (2008)]

# Electronic transport calculations in nanoscale systems

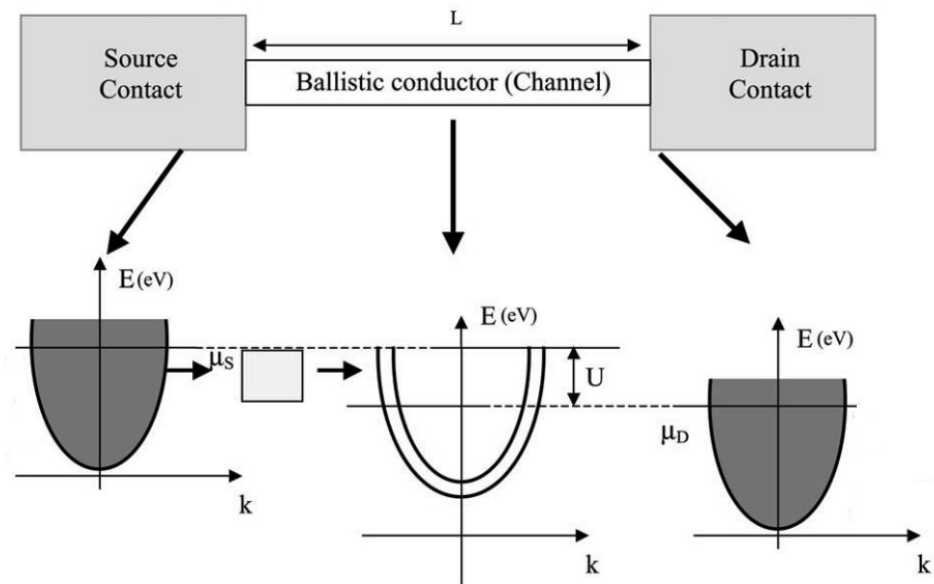
- This slide introduces:
  - Our methodology
  - 3<sup>rd</sup> part of my talk – our code TIMES
- Landauer theory (fig & equations to right)
- Non-equilibrium Green's function method (NEGF)
- Results presented today use:
  - TIMES (Transport in Mesoscopic Systems)
  - Our in-house code
  - G, S, T from H
- Currently: Landauer level only
  - Post-processing step to electronic structure
- Work in progress:
  - Self-consistent loop (will discuss briefly later)

$$i(E) = e/h \times T(E, V) [f_L(E) - f_R(E)]$$

$$I = \int i(E) dE$$

$$f_L(E) = \frac{1}{1 + \exp\left(\frac{E - E_f}{KT/q}\right)}$$

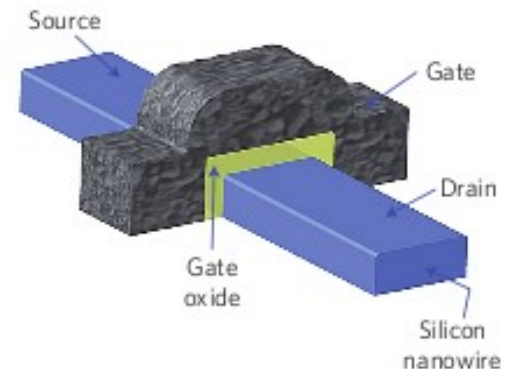
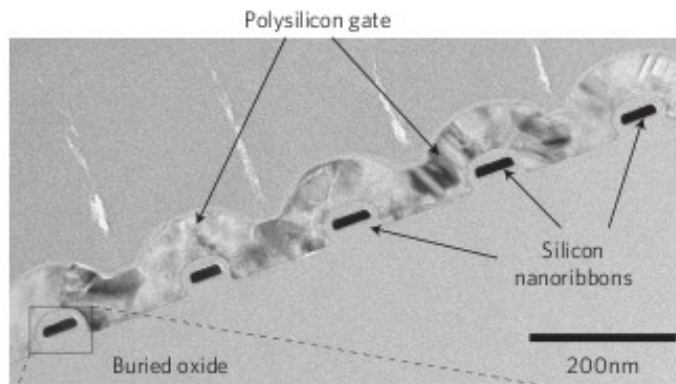
$$f_R(E) = \frac{1}{1 + \exp\left(\frac{E - E_f - qV_{ds}}{KT/q}\right)}$$



# Junctionless Si Nanowire Transistor

# Junctionless Si Nanowire (SiNW) Transistor

- J.-P. Colinge group, Tyndall [Colinge *et al*, Nature Nanotechnology, 5, 225 (2010)]
  - Experimental realization of junctionless Si nanowire (SiNW) transistor
    - “Gated resistor”: no junctions, doping gradients needed (fig. below right)
    - Key: Small cross-section
      - Multi-gate structure depletes highly-doped channel
      - Can turn off device
    - Expt. & theory: good short channel characteristics
    - Micron channel length scale – *not nano-device*
- Present work: Simulate realistic nano-device (1 nm thick; 3 nm long) with gating field
  - Predict I-Vds characteristics
  - Follow up our previous SiNW studies, [G. Fagas, J. C. Greer, Nano Lett., 2009; F. Murphy-Armando, G. Fagas, and J. C. Greer, Nano Lett., 2010]



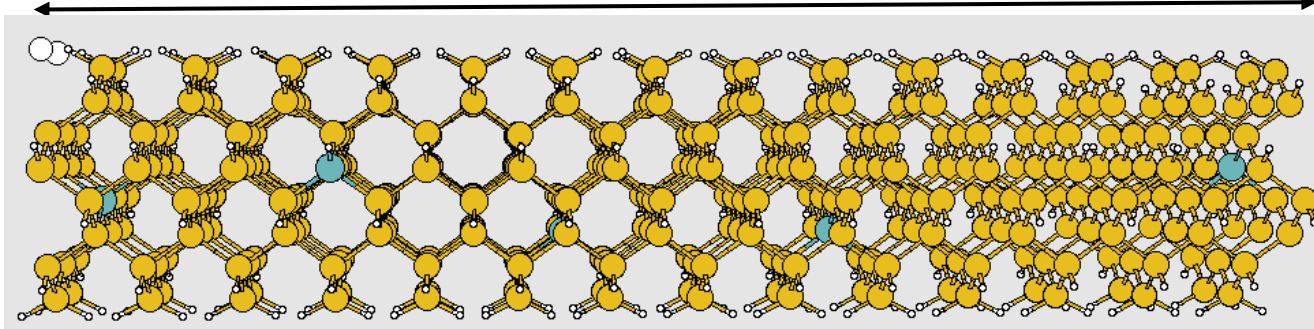
TEM (left) and schematic (right) of experimental junctionless SiNW transistor.  
Figures from [Colinge *et al*, Nature Nanotech., 5, 225 (2010)],

# SiNW Structure & Geometry

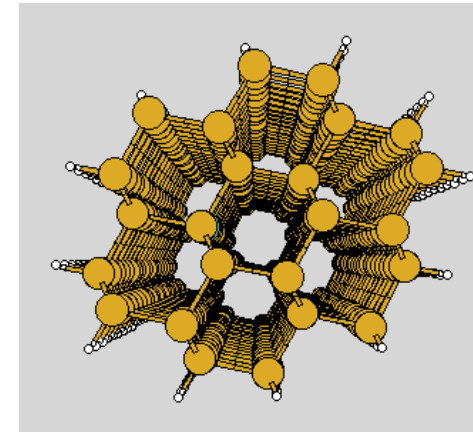
- Relaxed H-saturated [110] SiNW (below & right)

- Diameter = 1.15 nm
- Dopant atoms: As or P
- Structure from [G. Fagas, J. C. Greer, Nano Lett., 2009]

Supercell = 7.7 nm (~800 atoms)



Gated length = 3.1 nm

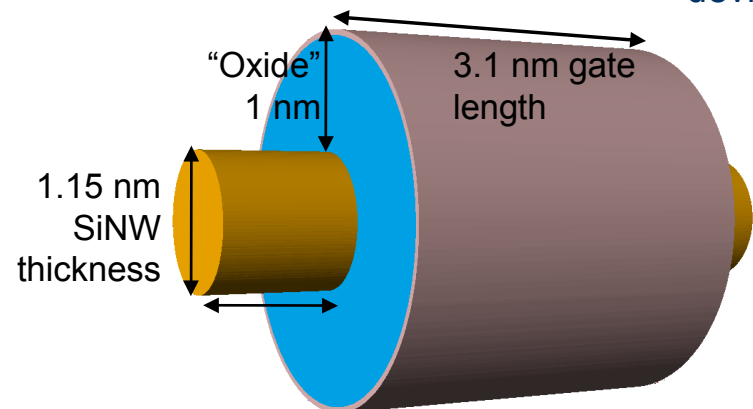


Cross section

Schematic of gated simulated device

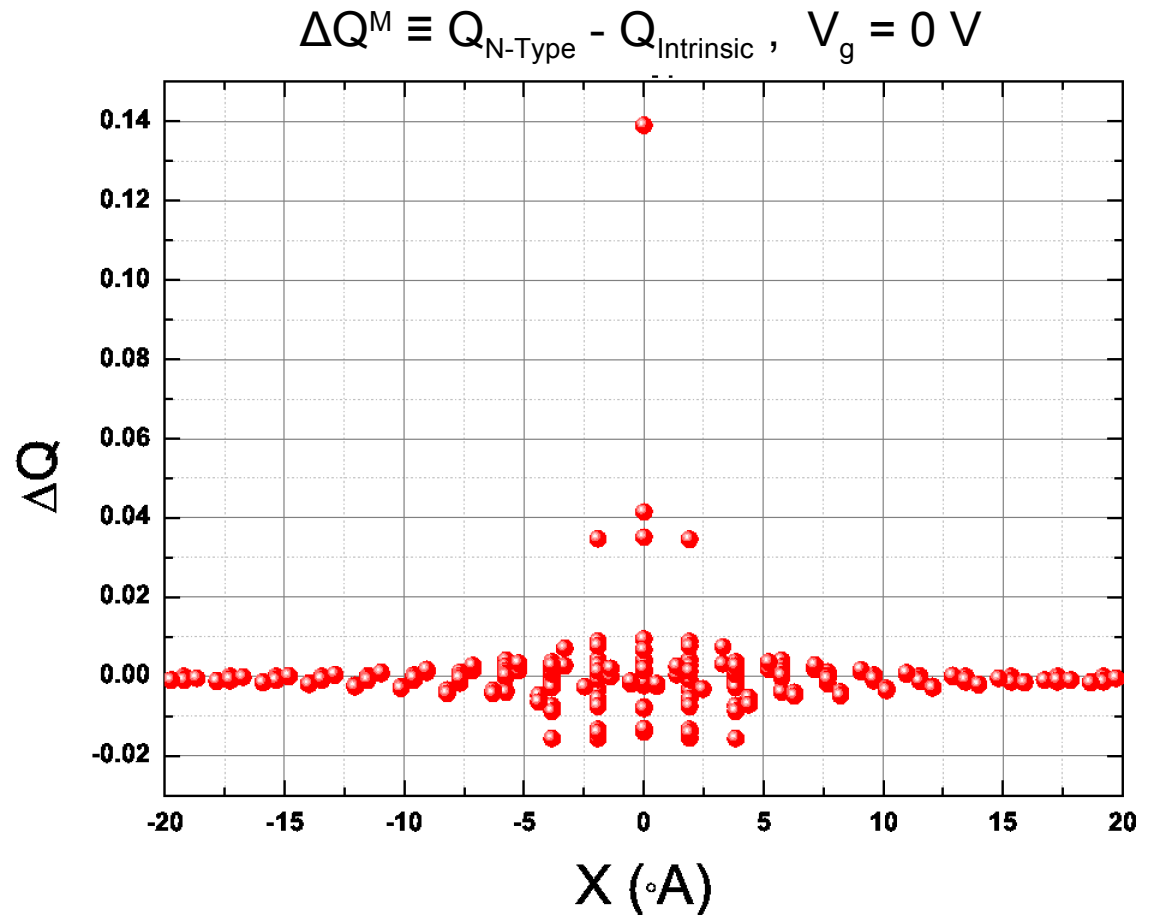
- Simulated GAA junctionless transistor (right):

- “Oxide” thickness 1 nm – continuum dielectric,  $\kappa$
- Gate length = 3.1 nm
  - Fixed point charges ( $> 3 \times 10^3$ , spaced 1 Å)
- Natural length = 0.76 nm



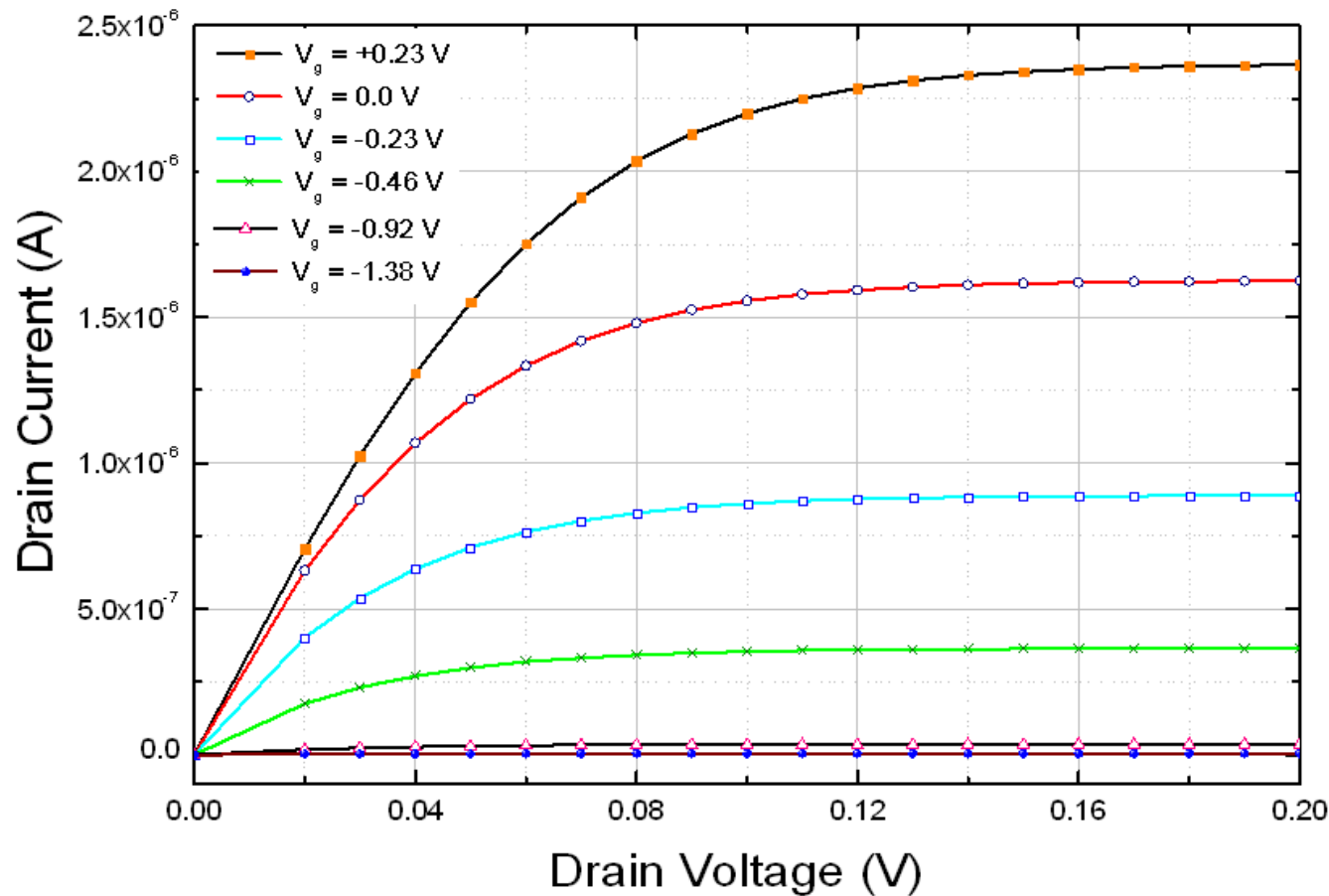
# Carrier delocalization in doped SiNW channel

- Mulliken charge difference,  $\Delta Q^M$ 
  - Charge de-localizes over radius  $\sim 1$  nm !
  - Comparable to gate length
- Result *independent* of  $T_e$  (!?)
  - Explained by combination of:
    - Si dielectric constant
    - Carrier confinement to thin nanowire



- **Result has ramifications for device design**
  - *Junctionless* design robust against dopant fluctuations
  - Conversely, *junctions* harder to achieve

# $I$ - $V_{ds}$ characteristic: N-type junctionless device

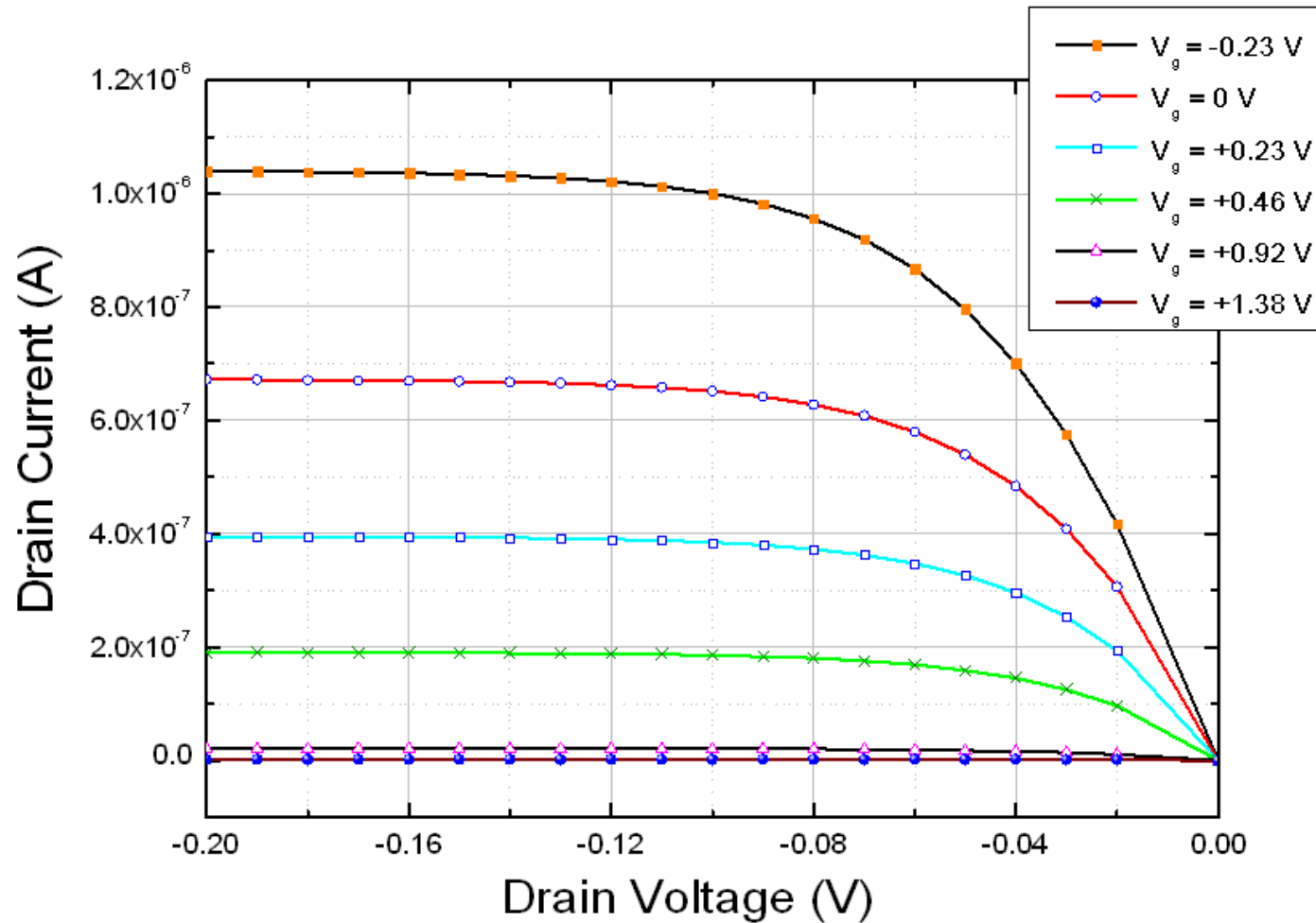


- **Device turns off**
  - Our primary result
  - Validated with E shift
- Tunneling could have increased source-drain leakage
  - Find  $I_{\text{off}} / I_{\text{on}} < 10^{-6}$
- Curves show current saturation, like conventional device
  - Lack of overlap between bands for large bias
  - Kim *et al.* [IEEE Trans. Nanotechnol., 2008]
- Gate voltage is estimate only

[L. Ansari, B. Feldman, G. Fagas,  
J.-P. Colinge, and J. C. Greer.

To appear in *Appl. Phys. Lett.* arXiv:1003.4631]

# I- $V_{ds}$ characteristic: P-type junctionless device



# Junctionless CNT Transistor

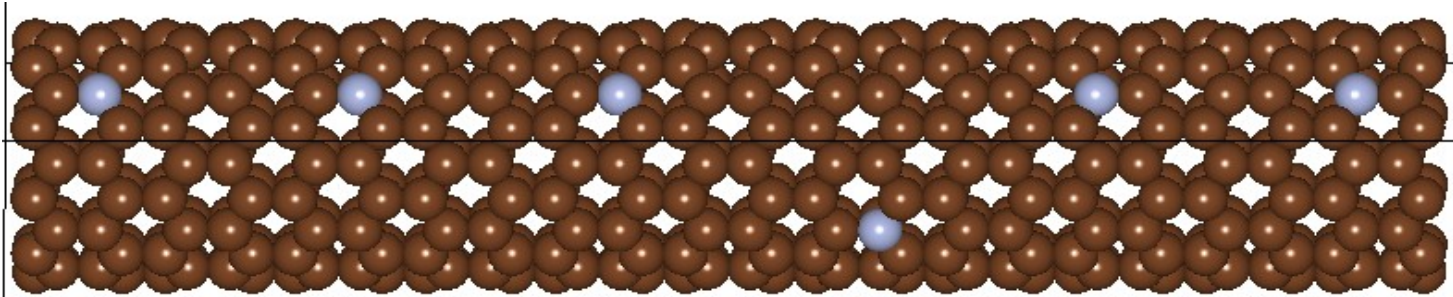
# CNT Structure

Simulation supercell: 440 atoms

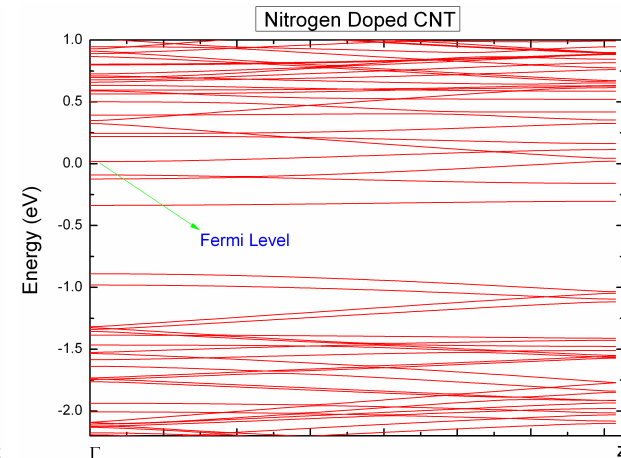
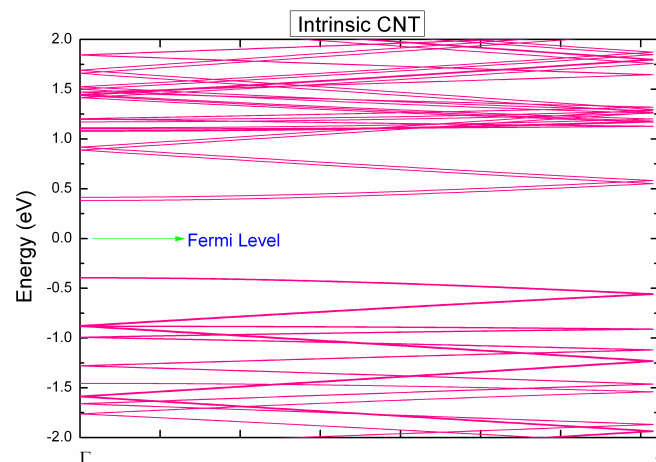
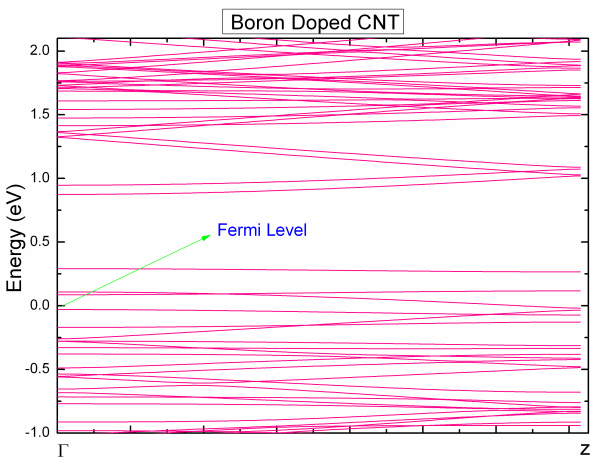
Gated length = 3.7 nm

4.65 nm

Doped with B or N

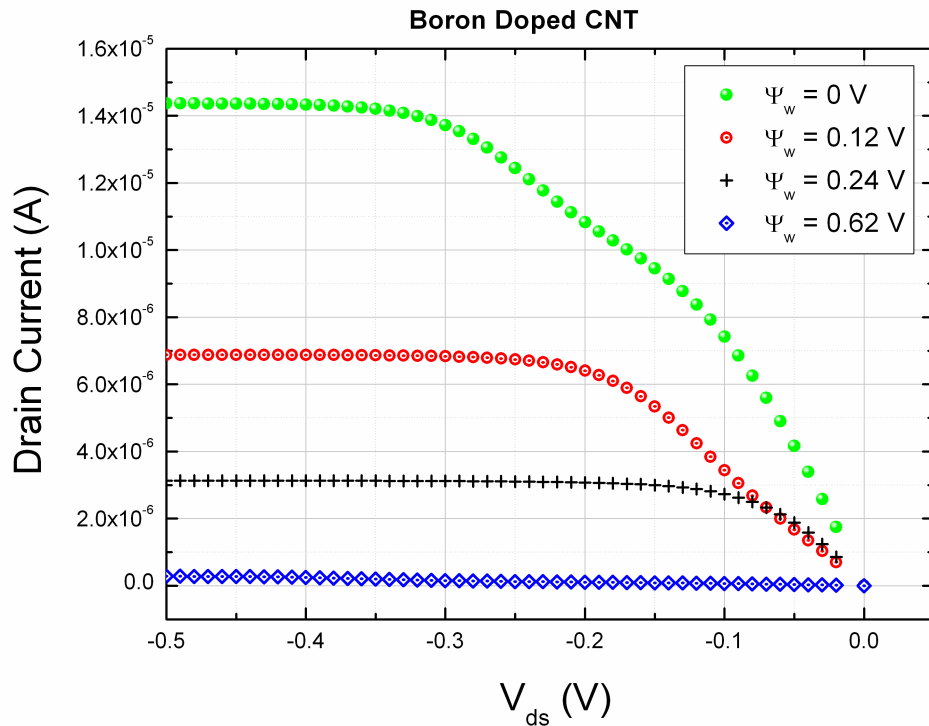


Band structures of P-type, undoped, and N-type SWCNT

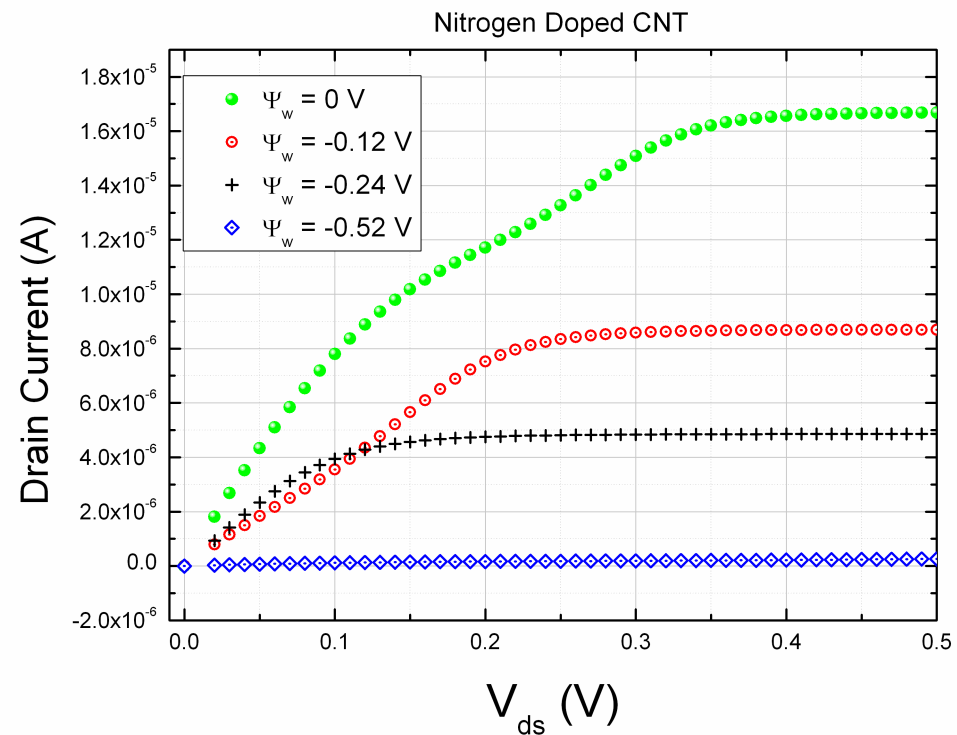


# Results

## 1.4% boron-doped SWNT (P-type)



## 1.4% nitrogen-doped SWNT (N-type)



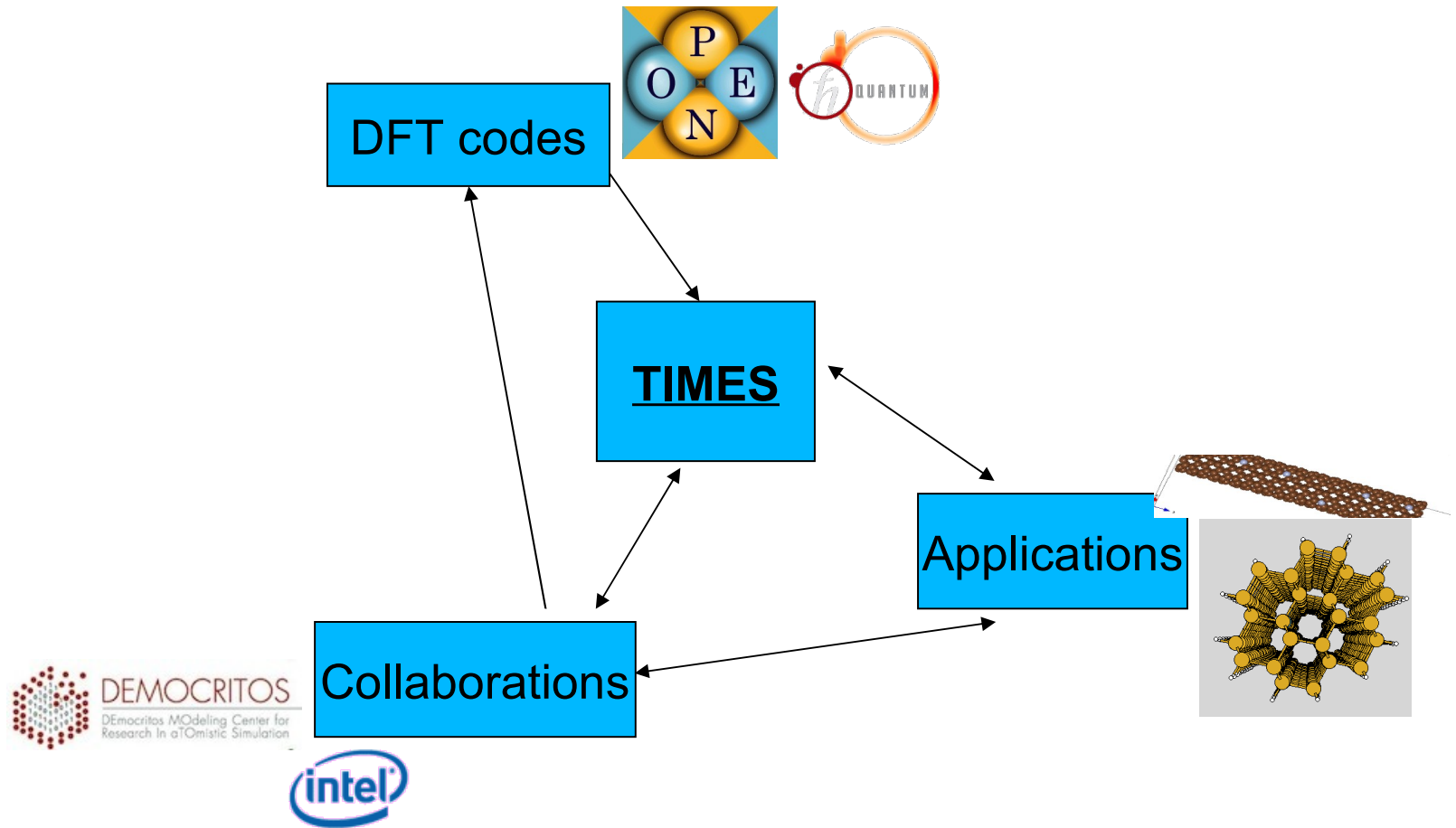
*Work in progress.* This slide:  $\Psi$  = potential *on* CNT, not gate.

[L. Ansari, B. Feldman, G. Fagas,  
J. C. Greer, S. Park, S. Shankar, forthcoming]

# **NEGF Code TIMES**

## **(Transport in Mesoscopic Systems)**

# TIMES in Tyndall's research



# TIMES NEGF code

- Modular - Currently, 3 e<sup>-</sup> structure codes
  - OpenMX (JAIST)
  - Quantum Espresso / pwscf (SISSA)
  - DFTB+ (Frauenheim *et al.*)
- Improvements to TIMES (in progress)
  - Self-consistent iteration & bias calculations
    - Retaining modularity
  - Parallelization (energy, k-space, algorithm)
    - Periodic boundary conditions
  - Probably extend to interface with more codes

## Multi-stage simulation: Growth / Synthesis to Transport

**1. Synthesis** ▪ Ab-initio relaxation on systems with many hundreds of atoms using massively-parallel computing environments.

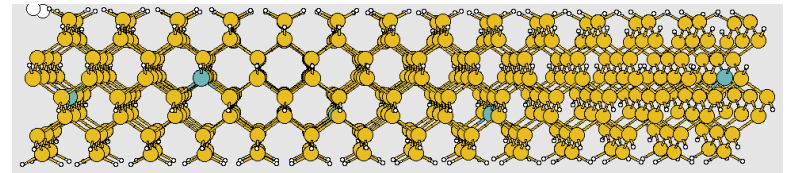
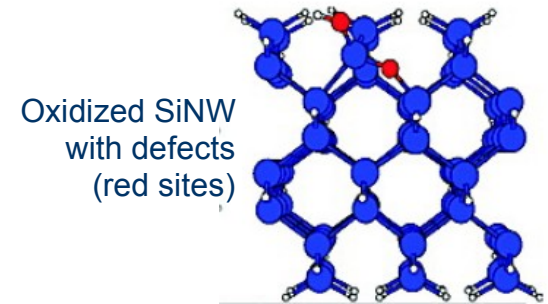
**2. Electronic Structure** ▪ TIMES suite is modular, interfacing with multiple popular open-source electronic structure codes, particularly Density Functional Theory (DFT) codes.

**3. Conduction** ▪ Non-equilibrium Green's function method (NEGF) calculations of nano- and meso-scale system conductance.

**4. Temperature** ▪ Research underway to incorporate electron-phonon scattering lifetimes for realistic simulations of scattering-limited transport in high-temperature operating environments.

# TIMES as a benchmarking tool

- G. Fagas, B. Feldman, D. Sharma, L. Ansari, J. C. Greer
  - Forthcoming paper – work in progress
- Systems:
  - SiNW junctionless transistor (right below)
  - Oxidized SiNW with defects (right top)
- DFT results with:
  - DFTB+
  - OpenMX
  - Quantum Espresso
- Also forthcoming: demonstration of SCC results



SiNW junctionless transistor (from previous work)

# Summary & Conclusions

# Summary & Conclusions

- End of Si technology roadmap
  - Nanowire devices proposed
  - Short channel effects are a serious challenge
- 3 nm junctionless SiNW transistor
  - At this scale, junctioned MOSFETs may be hampered by dopant delocalization
    - Ultra-shallow junctions also hard to fabricate
  - Predicted junctionless device can turn off at this scale
    - Dopant delocalization makes *more robust* to dopant fluctuations
- CNT transistor
- TIMES

