



### **A multilevel nanowire technology**

Thomas Ernst ([thomas.ernst@cea.fr](mailto:thomas.ernst@cea.fr))  
CEA-Leti, Grenoble

3D CMOS nanowire matrices and 2D thin film technologies recently developed enable not only sub-22nm CMOS device scaling but also ultimate co-integration of novel functionalities [1-3].

For CMOS scaling, Silicon-On-Insulator (SOI) or innovative Silicon-On-Nothing (SON) based 3D nanowires are proposed with common or independent gates. Ultra-low static consumption as well as high driving current were achieved thanks to 3D stacked Gate-All-Around (GAA) nanowire channels.

The top-down nanowire techniques also open up new opportunities for hybridizing CMOS with novel functionalities such as 3D memories, nano-oscillators and bio nano-sensors.

[1] T.Ernst et al. IEDM 2006, 2008

[2] A. Hubert et al, IEDM 2009

[3] K. Tachi et al, IEDM 2009