



***Les Séminaires de la Fondation
“Nanosciences aux limites de la Nanoélectronique”***

**Jeudi 23 Septembre 2010
à 16h**

Philip Wong

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Department of Electrical Engineering - Stanford University
Chaire d'Excellence de la Fondation Nanosciences



Présentera un séminaire intitulé :

**Carbon Electronics :
From Material Synthesis to Circuit Demonstration**

Vous êtes tous cordialement invités au pot qui suivra la présentation.

**Amphithéâtre 15 de l'école PHELMA-Polygone
(anciennement ENSERG)
23 rue des Martyrs – 38000 Grenoble**

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Carbon Electronics : From Material Synthesis to Circuit Demonstration

This year marks the 13th anniversary of the first publication of the carbon nanotube transistor. While there have been significant accomplishments in fundamental understanding and discovery, the engineering work that is required to harness carbon nanotube into useful technologies is just beginning.

This presentation reviews recent progress in carbon nanotube electronics, focusing on digital logic applications including the transistor and the interconnect wires. We will start with material synthesis using chemical vapor deposition and present a method for growing predominantly aligned carbon nanotubes over hundreds of microns over full 4-inch wafers. Techniques to transfer these carbon nanotubes to arbitrary substrates will be presented. This enabled the development of a variety of applications including three-dimensionally integrated carbon nanotube circuits. This is followed by device fabrication and circuit demonstration, showing rail-to-rail, cascadable logic gates that point the way to large scale integrated circuits. We will present some recent advances in mitigating the impact of metallic carbon nanotubes for transistor applications and forming good metal to carbon nanotube contacts. Compact device models have been developed for circuit and system-level performance estimation and circuit design. The models are relatively robust and have been used successfully in many academic research groups independent of our involvement. Finally we will conclude with recent results of an experimental demonstration of GHz operation of ring oscillator digital CMOS circuits using metallic carbon nanotube and graphene as interconnects.

Biography

Prof. Wong worked for 16 years at IBM Research, New York. As Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology.

Consequently, he worked in a broad range of other areas at IBM: CCD and CMOS image sensors, double-gate/multi-gate MOSFET, device simulations for advanced/novel MOSFET, strained silicon, wafer bonding, ultra-thin body SOI, extremely short gate FET, germanium MOSFET, carbon nanotube FET, and phase change memory.

His present research covers a broad range of topics including carbon nanotubes, semiconductor nanowires, self-assembly, exploratory logic devices, nanoelectromechanical devices, novel memory devices, and biosensors.

Philip Wong joined Stanford University in 2004 where he is Professor of Electrical Engineering. He also holds a Chair of Excellence at the Nanosciences Foundation since 2007. This seminar will be an excellent opportunity to know more about his research interests and his scientific projects and interactions in Grenoble.

H.-S. Philip Wong

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